REMARKS

Reconsideration of the instant application is respectfully requested. The present amendment is responsive to the Office Action of February 7, 2005, in which claims 1-18 are presently pending. Of those, claims 1 and 10 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent 5,770,484 to Kleinhenz. Claims 1, 2, 10 and 11 also stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Application Publication 2004/0147074 by Sell, et al.

In addition, claims 3, 4, 12 and 13 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Sell, in view of the publication entitled "Handbook of Plasma Processing Technology" by Rossnagel, et al. Finally, claims 5-9 and 14-18 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Sell, in view of the publication entitled "Silicon Processing for the VLSI Era, Volume 4: Deep-Submicron Process Technology" by Wolf. For the following reasons, however, it is respectfully submitted that the application is now in condition for allowance.

Independent claims 1 and 10 have been amended as indicated above to more particularly point out that the single etch step is sufficient to etch through the bulk silicon layer to a depth corresponding to a desired deep trench depth. Support for this amendment may be found at least in paragraphs [0015], [0020] and [0021] of the electronically filed specification, as well as in Figure 5.

A review of Figure 4 and column 3, line 40 through column 4, line 35 of the Kleinhenz reference reveals that although a single etch is used to etch though an SOI layer (120), a buried insulator layer (110) underneath the SOI layer, and a bulk silicon layer (100) beneath the buried insulator, the extent to which the bulk silicon layer is etched by this single step is minimal. As is specifically stated in column 4, lines 12-17 of Kleinhenz:

"Referring to FIG. 4, a photoresist mask (not shown) typically having a resist thickness in the range of 0.5 to 2 microns is used to etch an opening through the mask layers 150, 140 and 130 and continue etching through the device silicon layer 120 and *slightly pass the buried oxide layer 110 into the substrate 100.*" (Emphasis added)

In other words, the slight degree to which the first Kleinhenz etch penetrates the substrate 100 is insufficient, by itself, to create the necessary depth for a deep trench structure. It is not until after a silicon nitride deposition (170) (Figure 5) is implemented that a separate etch is then used to actually define the deep trench 200 as shown in Figure 6 of Kleinhenz. As such, the claims as presently amended have overcome the §102(b) rejections based on Kleinhenz.

Furthermore, the Applicants also traverse each the §102(e) rejections based on the Sell publication for the reason that Sell fails to teach or suggest the claimed method of implementing a single etch step to etch through an SOI layer, a buried insulator layer underneath the SOI layer, and a bulk silicon layer beneath the buried insulator layer to a depth corresponding to a desired deep trench depth. A review of Figure 8 and paragraph [0076] of Sell plainly reveals that the initial etching step only etches through the active SOI layer 47 and the buried insulator layer 46, **stopping** on the bulk silicon layer 41. More particularly, the last two sentences of paragraph [0076] of Sell state that:

"Then, the active Si layer 47 is etched by plasma etching using HBr/NF_3 and the buried oxide layer 46 is etched by plasma etching using CHF_3/O_2. The parameters of this etching step are such that the trenches are only etched as far as the lower end of the buried oxide layer 46."

Thus, not only does the initial Sell etch step fail to etch beyond the buried oxide layer 46 and into the bulk silicon layer 41, the process of etching first through the SOI layer 47 and then through the BOX layer 46 is actually two discrete steps using two separate chemistries (i.e., HBr/NF_3 to etch through SOI layer 47 and then CHF_3/O_2 to etch

through BOX layer 46). Furthermore, paragraph [0077] of Sell confirms that there is still a third discrete etch step and chemistry that is needed to define the deep trench depth within the bulk silicon layer 41:

"Then, the capacitor trenches 45 are etched down to a depth of 5μm by plasma etching using HBr (sic)/NF_3, as illustrated in Fig. 9."

Accordingly, it is respectfully submitted that the claims as presently amended have overcome each of the §102(b) rejections based on Kleinhenz, the §102(e) rejections based on Sell (and therefore each of the §103 rejections as well), and it is respectfully requested that the same be withdrawn.

For the above stated reasons, it is respectfully submitted that the present application is now in condition for allowance. No new matter has been entered and no additional fees are believed to be required. However, if any fees are due with respect to this Amendment, please charge them to Deposit Account No. 09-0458 maintained by Applicants' attorneys.

Respectfully submitted,
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